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TEM investigation on top Si layer and buried oxide layer in silicon wafer implanted with low dose at low energy

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Microstructures of as-received Si wafers prepared by Separation by Implanted Oxygen (SIMOX) techniques have been investigated by means of high-resolution transmission electron microscopy (TEM) with interest mainly in the top Si layer and the buried oxide (BOX) layer which were developed in the production process. Cross-sectional TEM and HRTEM micrographs clearly reveal the existence of thermally produced oxide layers over the Si top interfaces in both the protectively capped and uncapped Si wafers implanted with different doses of oxygen ions at low fixed energy level, and before the annealing process. The thickness of the top Si layer and the BOX layer have been measured and it is apparent that the thickness of these layers relates to the thermally grown oxide layer covering the top Si layer. The TEM analysis allows an understanding and explanation to be made of the different deposition and growth processes of the thermal oxide layers that cover the top Si layers. Copyright © 2004 John Wiley & Sons, Ltd.

INTRODUCTION

Separation by **Im**planted **O**xygen (SIMOX) techniques have been used for producing a buried oxide layer to provide a technical advantage over bulk Si. SIMOX is the most widely used commercial silicon on insulator (SOI)[1–9] process. It has been reported that a low oxygen dose ion implantation process, followed by a high-temperature annealing treatment could synthesize a thin top Si layer and a thin buried oxide layer (the BOX layer).[1–5,7] These thin layers have been 'designed into' recent production techniques to develop the optimum properties and minimize production costs.[4,5]

In this study, the microstructure of SIMOX wafers has been investigated using cross-sectional TEM and HRTEM techniques to observe microstructural changes after the annealing process. SIMOX wafers were produced with a low-dose oxygen at low implantation energy. In addition, the interface on top of the Si layer was characterized from SIMOX treated samples with and without chemical protection before the fixed high-temperature annealing in order to understand the mechanism of microstructural changes taking place.

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EXPERIMENTAL PROCEDURES

SIMOX wafers were received from Prof. S. Seraphin, University of Arizona, Tucson, USA, and prepared by the methods given in Refs 4 and 5. (100) Silicon wafers were implanted using an Ibis 1000 high-current oxygen implanter at 65 keV and 500 °C. Oxygen doses of 3.0, 3.5, 4.0 and $7.0 \times 10^{17}O^{+}/cm^{2}$, were employed for specimen preparation. To compare Si wafers having a surface protected from thermal oxidation, a set of the same oxygen-dosed wafer samples were coated by tetraethylorthosilicate (TEOS, $Si(OCH_2CH_3)_4$). Subsequently, all of the TEOS capped (coated) and uncapped wafers were annealed at 1350 °C for 4 h in an Ar + 1% O_2 atmosphere.

Cross-sectional XTEM samples of SIMOX wafers were prepared using standard techniques (Gatan Co., USA). The preparation techniques have been described in detail elsewhere.[10] The XTEM samples were then examined using TEM, in a JEOL 2010 instrument operated at 200 keV, having a point resolution of 0.19 nm. High-resolution transmission electron microscopy (HRTEM) techniques were used to observe the top Si interface and the BOX layer behaviour and thickness.

RESULTS AND DISCUSSION

General microstructure

Figures 1 and 2 show the overall microstructure of Si wafers implanted with low oxygen dose at low energy of uncapped and capped TEOS, respectively. All the Si wafers changed

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Figure 1. A set of XTEM micrographs of samples implanted with doses of 3.0, 3.5, 4.0 and 7.0×10^{17} O^+/cm^2 without the TEOS protective cap.

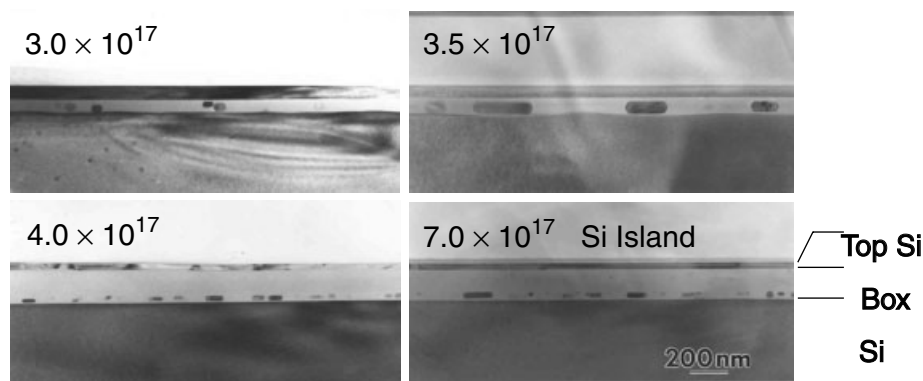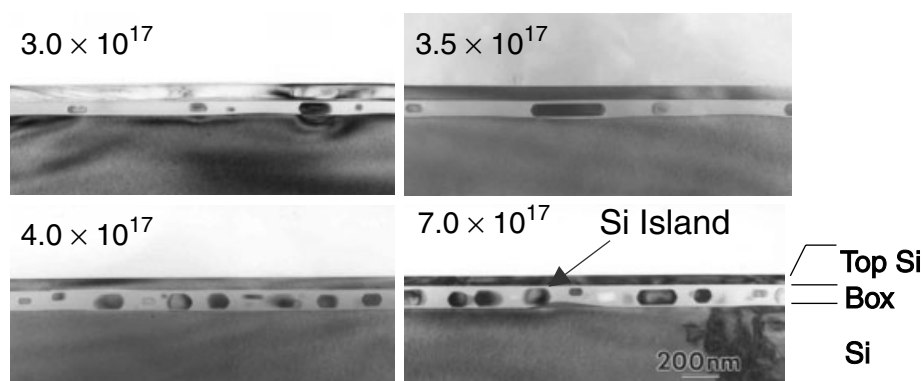**Figure 2.** A set of XTEM micrographs of samples implanted with doses of 3.0, 3.5, 4.0 and 7.0×10^{17} O^+/cm^2 with the TEOS protective cap.

their microstructures by forming separate layers; a top Si layer, and the BOX layer in both capped and uncapped samples. The BOX layers are an amorphous form of SiO_2. Previous reports suggest these layers were formed sharply after passing through the annealing process.[1–8] Si inclusions or islands can be seen in all samples. The size of Si islands in the capped samples is larger than in the uncapped wafers, indicative of a growth process.

Table 1 shows the measured thickness of the top Si and BOX layers for each oxygen dose in both the TEOS uncapped and capped samples, a separate oxide layer having formed for all oxygen doses. The thickness of the BOX layer is seen to increase with increase of oxygen dose. The BOX layer thickness is considered to depend on the amount of excess oxygen available. Si islands can be observed by TEM in all

samples with the Si islands in the BOX layer of the uncapped samples being larger than those in the capped samples.

Investigation of the upper interface of the top Si layer

Figure 3(a) and (b) reveals the thermal oxide layers present in both types of samples. The thermal oxide/epoxy interface can be identified from the dark line present in the lower-magnification XTEM image. The reactions that allow formation of the thermal oxide layers are expected to differ for each type of sample. The thermal oxide from the uncapped samples should derive from Si at the surface reacting with free oxygen present during the annealing process resulting in formation of amorphous SiO_2, as proposed in the chemical reaction in Eqn (1).[9]

Oxidation of Si:

$$Si(s) + O_2(g) \longrightarrow SiO_2(s) \qquad (1)$$

Excess oxygen can react with Si at the wafer surface during annealing until the reaction is complete. The thickness of the Si top surface should gradually decrease in the process of forming an amorphous layer of thermal oxide. The interface of the top Si/SiO_2 should present a more crystalline morphology since Si from the top Si layer is decreased. It has been reported that this thermal oxide layer has formed after a high-temperature annealing process[4,5] but supporting evidence has not been provided. Other authors report

Table 1. Thickness of top Si and BOX layer

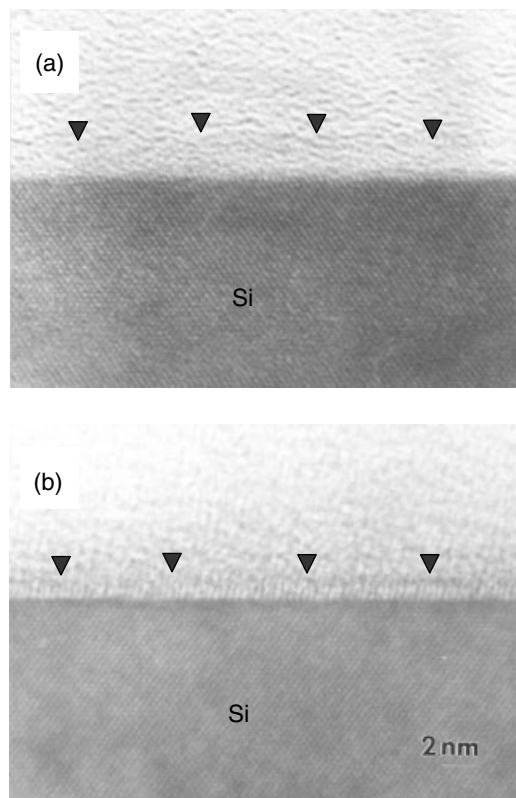| Oxygen dose ($\times 10^{17}$ O^+/cm^2)	Top Si layer (nm)		BOX layer (nm)	
	Uncapped sample	Capped sample	Uncapped sample	Capped sample
3.0	72	91	69	73
3.5	64	73	91	87
4.0	35	66	173	111
7.0	35	54	164	116

Figure 3. Typical HRTEM images of top Si/thermal oxide interfaces in $4.0 \times 10^{17} O^+/cm^2$ dose samples; (a) the uncapped and (b) the capped sample. The thermal oxide layer can be seen above the top Si interface in both samples.

the existence of a thermal oxide layer having $\sim$20–50 nm thickness above the top Si interface of an uncapped sample at the same doses of 4.0×10^{17} and $7.0 \times 10^{17} O^+/cm^2$.[1,2]

However, the thermal oxide layer observed in the capped TEOS samples should be formed from the reaction of TEOS with free oxygen during the annealing process, as explained in Eqn (2). When this reaction occurs, the Si layer thickness should not be decreased because amorphous SiO_2 from the reaction is left above the top Si surface as shown in the chemical reaction in Eqn (2). This decomposition reaction is commonly used to grow SiO_2 film at temperatures as low as 400 °C when oxygen containing 4% ozone is used.[11]

Decomposition of organic, TEOS:

$$Si(OCH_2CH_3)_4 + 12O_2 \longrightarrow SiO_2 + 8CO_2 + 10H_2O \quad (2)$$
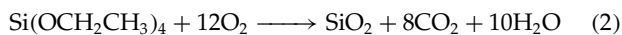
Lattice image of Si island in BOX layer using HRTEM observation

Figure 4 shows an example of a lattice image of part of a Si island in a BOX layer in samples dosed at $4.0 \times 10^{17} O^+/cm^2$ capped with TEOS. It can be seen clearly that the lattice images of the Si islands are coincident with the lattice image of the top Si, and this lattice coincidence occurs in the Si wafer. This phenomena can be observed for all sample doses with and without capped TEOS, which suggests that the Si islands are created by diffusion of oxygen to nucleate on Si defects such as stacking faults or dislocations, giving amorphous SiO_2 in the BOX layer. The amount of oxygen
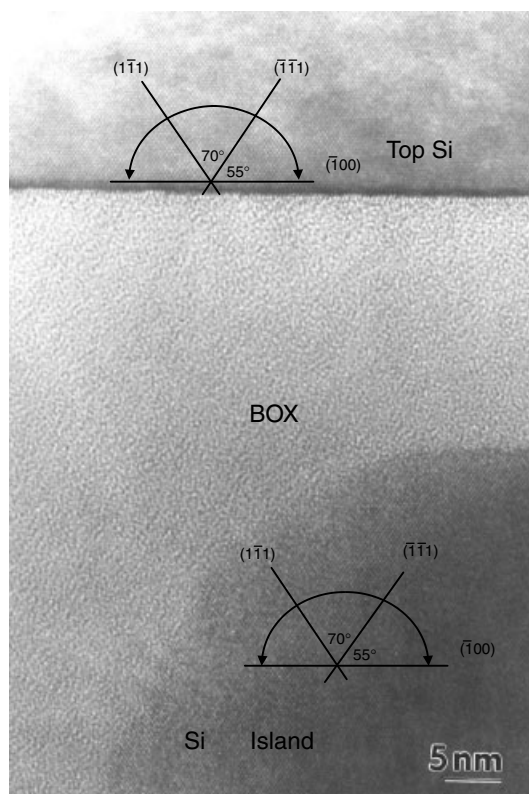

Figure 4. A typical HRTEM micrograph of the capped sample with dose of $4.0 \times 10^{17} O^+/cm^2$. Lattice images of the Si island and the top Si are coincident.

present for the reaction is limited, subsequently free Si in the BOX layer remains and realigns to have the same coincidence lattice as the adjacent Si wafer and the top Si. All Si islands observed by HRTEM in each of the SIMOX wafers of both types have this common morphology.

CONCLUSIONS

Microstructures of SIMOX samples prepared using low-dose (3.0, 3.5, 4.0 and $7.0 \times 10^{17} O^+/cm^2$) at low-energy (65 keV) ion implantation followed by annealing at 1350 °C for 4 h have been investigated using XTEM and HRTEM techniques. HRTEM micrographs clearly reveal the existence of thermally produced oxide layers over the Si top interfaces in both the protective TEOS capped and uncapped Si wafers. The thickness of the top Si layer was measured in all samples and it is considered that this thickness depends on chemical reactions in both types. Lattice coincidence of the Si island can help explain the mechanism of the BOX layer formation.

REFERENCES

1. Nakashima S, Izumi K. *J. Mater. Res.* 1993; **8**: 523.
2. Nakashima S, Izumi K. *J. Mater. Res.* 1992; **7**: 788.
3. Nakashima S, Izumi K. *J. Mater. Res.* 1990; **5**: 1918.

4. Johnson B, Tan Y, Anderson P, Seraphin S, Anc MJ. *J. Electrochem. Soc.* 2001; **148**: G63.

5. Jiao J, Johnson B, Seraphin S, Anc MJ, Cordts BF. *Mater. Sci. Eng.* 2000; **B72**: 150.

6. Van Ommen AH, Koek BH, Viegers MPA. *Appl. Phys. Lett.* 1986; **49**: 1062.

7. Li Y, Kilner JA, Chater RJ, Hemment PLF, Nejim A, Robinson AK, Reeson KJ, Marsh CD, Booker GR. *J. Electrochem. Soc.* 1993; **140**: 1780.

8. Stoemenos J, Margail J, Dupuy M, Jaussaud C. *Physica Scripta*, 1987; **35**: 42.

9. Mahajan S, Sree Harsha KS. In *Principles of Growth and Processing of Semiconductors*, McGraw-Hill: Singapore, 1999; 298.

10. Alani R, Jones J, Swann P. In *Mat. Res. Soc. Symp. Proc.*, vol. 199, Anderson R (Ed). Materials Research Society: 1990; 85.

11. Ghandhi SK. In *CLSI Fabrication Principles: Silicon and Gallium Arsenide*, Wiley: NY, 1994; 528.